In the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Cancelled)

2. (Currently Amended) The circuit layout configuration of claim [[1]] 8, wherein ~~a gate of each of the sub-transistors forming the first transistor and a gate of each of the sub-transistors forming the second transistor are connected in common,~~ gates of the eight first sub-transistor and the eight second sub-transistors are connected [[and]] so that the first transistor and the second transistor form a current mirror circuit.

3. (Currently Amended) The circuit layout configuration of claim [[1]] 8, wherein gates of the first sub-transistors ~~forming the first transistor~~ are connected ~~in common~~ to form a gate of the first transistor and gates of the second sub-transistors ~~forming the second transistor~~ are connected ~~in common~~ to form a gate of the second transistor.

4. (Original) The circuit layout configuration of claim 3, wherein the first and second transistors form differential input pair transistors of an operational amplifier.

5. (Currently Amended) The circuit layout configuration of claim ~~1, 2, 3 or 4~~ 8, wherein sources of the first sub-transistors ~~forming the first transistor~~ are connected ~~in common~~ and drains of the first sub-transistors ~~forming the first transistor~~ are connected ~~in common~~.

6. (Currently Amended) The circuit layout configuration of claim 5, wherein sources of the second sub-transistors ~~forming the second transistor~~ are connected ~~in common~~ and drains of the second sub-transistors ~~forming the second transistor~~ are connected ~~in common~~.

7. (Currently Amended) The circuit layout configuration of claim ~~1, 2, 3 or 4~~ 8, ~~further comprising a plurality of circuits, each comprising the first cell, the second cell, the third cell and the fourth cell and disposed axisymmetrically~~ wherein the first transistor comprises eight additional first sub-transistors, the second transistor comprises eight additional second sub-transistors, and the eight additional first sub-transistors and the eight additional second sub-transistors are arranged so as to be symmetrical with the eight first sub-transistors and the eight second sub-transistors with respect to a line of symmetry.

8. (New) A circuit layout configuration for matching two transistors, comprising:

a first transistor comprising eight first sub-transistors; and

a second transistor comprising eight second sub-transistors,

wherein the eight first sub-transistors and the eight second sub-transistors are arranged in a four by four matrix, the eight second sub-transistors occupy eight diagonal positions of the four by four matrix, and the eight first sub-transistors occupy positions of the four by four matrix that are not the diagonal positions.